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| EAST History |         | 7/18/2005   | 3:43 PM  |
|--------------|---------|---|--|
| BRS          | 18      | (test adj block) and encoder and (compensation adj circuit)                     | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 1       | S18 and termination   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 2073614 | on die termination adj circuit  | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 485     | S20 and (test adj block)  | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 0       | S21 and ((compensation or compensating or compensate or adjust3\$) adj circuit) | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 73      | S21 and (compensation or compensating or compensate or adjust3\$)               | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 37      | S23 and (encoder or encoding or encode)   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 470     | S20 and pvt   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 29      | S25 and (((test or testing) adj circuit)  | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 22      | S26 and (encode or encoder or encoding)   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 647902  | programmable adj on die termination adj circuit                                 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 2773    | S28 and (memory adj controller)   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 38      | S29 and (((testing or test) adj circuit)  | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 0       | S30 and fsm   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 52      | S29 and fsm   | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB 18-Jul-05 |
| BRS          | 4       | ("5134311"   "6087847"   "6384621"   "6424175").PN.                             | US-PGPUB; USPAT; USOCR 18-Jul-05                             |
| BRS          | 0       | ("6624659").URPN.   | USPAT 18-Jul-05  |

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| BRS | 78   | S29 and (finite adj state adj machine)                      | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |
| BRS | 2156 | S28 and processor and memory and<br>(memory adj controller) | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |
| BRS | 9    | S36 and megatransfers                                       | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |
| BRS | 1    | S36 and mega-transfers                                      | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |
| BRS | 2    | S36 and (mega adj transfers)                                | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |
| BRS | 11   | S37 or S38 or S39   | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |
| BRS | 192  | S28 and (code adj generator)                                | USPAT  | 18-Jul-05 |
| BRS | 23   | S41 and (memory adj controller)                             | US-PGPUB; USPAT; USOCR;<br>EPO; JPO; DERWENT;<br>IBM_TDB | 18-Jul-05 |